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Cost-effective SET-tolerant clock distribution network design by mitigating single event transient propagation

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It has been shown that clock distribution networks (CDNs) are becoming increasingly vulnerable to transient faults known as single event transients (SETs), owing to technology scaling [1]. In the deep submicron regime, CDNs contribute significantly to the chip-level soft error rate (SER) [2] and radiation particle strikes on the CDN can prove to be catastrophic [3]. Abnormal behaviors in the whole system may be generated if the clock signal is altered by radiation effects [4, 5]. To mitigate and avoid mistaken data latching or failure of the whole circuit system caused by SETs on the clock signal, efficient hardening techniques for the CDN should be proposed.

Although hardening techniques for sequential and combinational circuits have been studied extensively in the past, few research efforts have addressed the problem of radiation hardening in the CDN of an integrated circuit (IC). In the few existing hardened clock circuit designs, Dash et al. [3] introduced the triple modulo redundancy (TMR) and split-output single event upset (SEU)-tolerant inverter approaches in the clock regeneration circuit. The split-output-based hardened regenerator will bring about extra delay, reduce the voltage swing, change the duty cycle of the clock signal, and may produce a high-impedance state. Using the C-element technique, Mallajosyula et al. [6] implemented an SEU-hardened clock leaf driver. It can eliminate 90% of the SER due to the clock network according to their simulation, but extra delay will be caused by the introduction of the delay element. In addition, the pulse width of the SETs that can be filtered is strongly dependent on the delay element. All of the techniques in [3, 6] can only be applied at the leaf node of the CDN and they all suffer from large area overhead, high power consumption, and high complexity. Moreover, in [3, 6], only single event single transients (SESTs) [7] of hardened leaf node circuits were simulated and evaluated, whereas the charge sharing effect and application of these hardening techniques in actual CDN design were not mentioned.

In this paper, a cost-effective SET-tolerant CDN design is proposed. It consists of dual-in-and-dual-out (DIDO) inverters (buffers), which can effectively mitigate SET propagation. The SET mitigation technique used in our design can be applied

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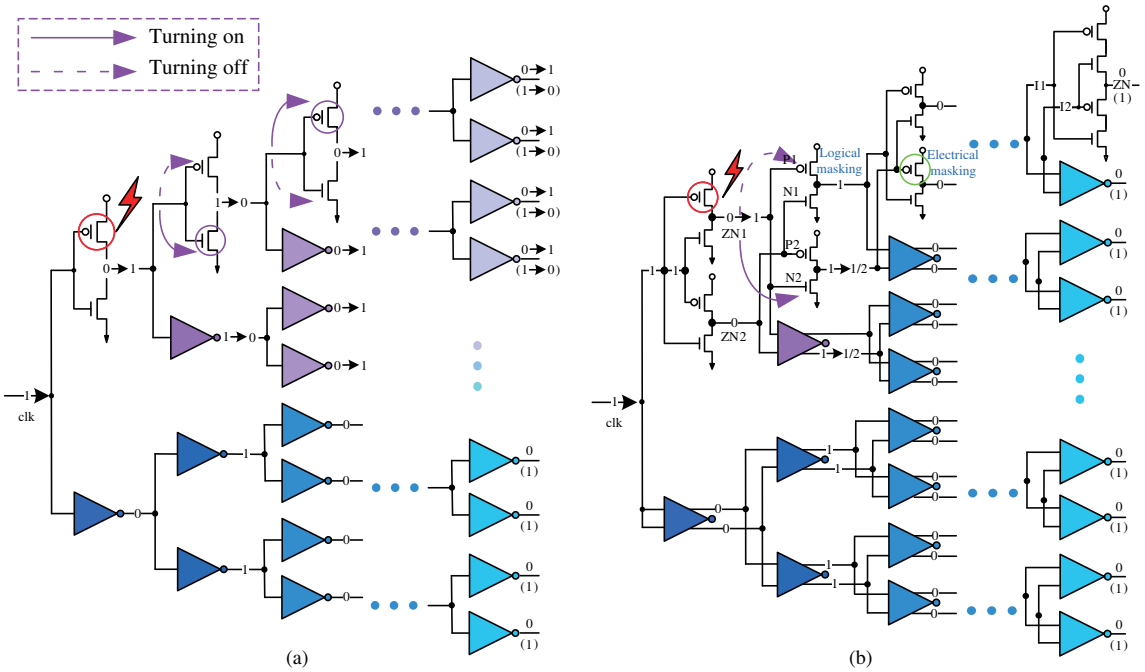

Figure 1 (Color online) Transient propagation in the (a) unhardened CDN; (b) SET-tolerant hardened CDN with DIDO and DISO inverters.

to a whole CDN or partial clock networks, including global and local networks. Moreover, the hardening technique is easy to realize and is suitable for CDNs with different topologies. The SET vulnerability and performance of the design are evaluated in depth.

SET in the unhardened CDN. In the unhardened CDN, a radiation particle striking on the clock inverter or clock buffer will generate some transient pulses, which will propagate to leaf nodes of the CDN. Depending on location of the struck inverter (or buffer) and the width and amplitude of the pulse, one or more soft errors will occur in the IC. In the worst case, the whole circuit will fail.

In a common unhardened CDN, those transistors in the off state may generate some transient pulses, which will propagate to the leaf node of the CDN. As shown in Figure 1(a), the transient from the PMOS in the off state will simultaneously turn on the NMOS and turn off the PMOS in its posterior inverter, and the transient from the NMOS in the off state will also simultaneously turn on the PMOS and turn off the NMOS in its posterior inverter. The transient turning off the same-type transistor in the posterior stage is an inherent logical masking, but the transient turning on the different-type transistor in the posterior stage counteracts it.

In real circuits, the transient may be masked by some logical signal, that is, the pulling-up (or pulling-down) induced by a turning-on action will be cancelled. However, when the masking signal is open, the transient still propagates, which means that the logical masking is dynamic. Therefore, it is necessary to exploit some static logical masking, which is an inherent feature of a circuit. The new logical masking technique means that the transient from the PMOS (or NMOS) in the off state no longer simultaneously turns on the NMOS (or PMOS) and turns off the PMOS (or NMOS) in its posterior stage.

Hardened CDN circuit design. The DIDO inverter (shown in Figure 1(b)) is proposed in this paper to meet the demand raised above. Similarly, the DIDO clock buffer can also be implemented. A schematic diagram of a hardened SET-tolerant CDN implemented with the DIDO inverter is shown in Figure 1(b). As shown in Figure 1(b), a transient generated at a PMOS in the off state will not simultaneously turn on the NMOS and turn off the PMOS in its posterior inverter (N1 and P1, N2 and P2). Thus, turning off the PMOS (P1) does not change its output value owing to the inherent logical masking, and turning on the NMOS (N2) does not cause a full-swing transient at its output voltage, because its corresponding pull-up PMOS (P2) is also in the on state. Owing to this rapid attenuation of the transient pulse amplitude, the electrical masking will be much more obvious as the transient propagates away. Thus, the transient no longer propagates to the leaf nodes of the CDN.

During normal operation, the DIDO inverter works as a common inverter. The two inputs of

the DIDO inverter are the same, and its two outputs are also the same.

Another kind of inverter with two inputs and one output (shown in Figure 1(b)) is introduced to realize the connection between the DIDO inverter (buffer) and sequential elements such as D flip-flops (DFFs). This kind of inverter, which is called a dual-in-and-single-out (DISO) inverter, is used as the last level clock inverter in the CDN. If the sequential elements are hardened by the dual interlocked storage cell (DICE) technique, this kind of inverter (buffer) will not be necessary.

In our study, a case circuit was used to verify the SET vulnerability of the SET-tolerant CDN. The whole design was implemented with 65 nm bulk CMOS technology. For comparison, an unhardened CDN with common inverters of the same case circuit was also implemented.

Results and discussion. According to the investigation of Seifert [2], for an FF-based design, the contribution due to radiation-induced clock jitter is less than 2% of the total clock path SER. Therefore, influence of the radiation-induced clock race on the hardened and unhardened CDNs of the case circuit is comparatively studied in this paper. All simulations were performed at 500 MHz. The SEST simulation results indicate that SETs appearing at leaf nodes of the proposed SET-tolerant CDN are reduced significantly. The probability of capturing SETs at leaf nodes of the SET-tolerant CDN caused by SEST occurring at the DIDO inverters because of radiation-induced clock race is 0%. However, this ratio increases to 49.19% in the unhardened CDN. If an SET occurs at the first-level unhardened clock inverter, there is a probability that this SET will propagate to all leaf nodes, depending on the amplitude and duration of the SET. Moreover, the SET-tolerant CDN is immune to the single event double transients (SEDTs) occurring between two DIDO inverters. Although there is a possibility that SEDTs occur in one DIDO inverter, numerical simulations using TCAD indicate that the probability of SEDTs in one DIDO inverter is low, and the SEDTs propagating to the leaf node can be filtered or quenched. Moreover, the SEDT in one DIDO inverter can be mitigated by layout techniques such as guard rings and guard drains.

To further verify the SET mitigation technique for CDNs proposed in our paper, we designed a test chip with 130 nm bulk CMOS technology. Heavy ion broad-beam irradiation experiments were performed on the test chip at the Heavy Ion Research Facility in Lanzhou (HIRFL), China. The cross-section of each test chain induced by SETs on the clock tree was measured for Bi particle irradiation at normal incidence. The cross-sections of the two test chains with the SET-tolerant clock tree are 0, and the cross-sections of the two test chains with the unhardened clock tree are 7.5 μm^2/bit and 3 μm^2/bit respectively. This further verifies the SET mitigation technique for CDNs proposed in our paper.

Comparisons in terms of area, timing, and power between the two designs of the case circuit with the SET-tolerant CDN and unhardened CDN were performed. The results show that the design with the SET-tolerant CDN suffers from a small area penalty. The overheads of transition and delay time on the longest clock path are only 41.565 ps and 44.045 ps, respectively, and the power penalty is acceptable.

Conclusion. In this paper, a cost-effective SET-tolerant CDN design by mitigating SET propagation is proposed. The proposed SET-tolerant hardened CDN significantly reduces the probability of SET due to radiation-induced clock race propagation to leaf nodes, and suffers from small area and power penalties. Meanwhile, the timing performance of the hardened CDN is changed slightly. Moreover, the hardening technique involved in our SET-tolerant CDN design can be used to conveniently implement CDNs with different topologies of arbitrary design.

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