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Flip-flops soft error rate evaluation approach considering internal single-event transient

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Abstract The internal single-event transient (SET) induced upset in flip-flops is becoming significant with the increase of the operating frequency. However, the conventional soft error rate (SER) evaluation approach could only produce an approximate upset prediction result caused by the internal SET. In this paper, we propose an improved SER evaluation approach based on Monte Carlo simulation. A novel SET-based upset model is implemented in the proposed evaluation approach to accurately predict upsets caused by the internal SET. A test chip was fabricated in a commercial 65 nm bulk process to validate the accuracy of the improved SER evaluation approach. The predicted single-event upset cross-sections are consistent with the experimental data.

Keywords soft error rate, Monte Carlo, internal SET, single-event upset, flip-flops

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1 Introduction

Technology scaling has increased the susceptibility of flip-flops to single-event upset (SEU) [1,2]. Reduced nodal capacitances and lower supply voltages decrease the critical charge that causes SEU. In addition, higher operating frequencies make the overall SER of flip-flops increase significantly [3,4]. The internal SET induced upset described in [3] is responsible for the frequency dependence of error rate. However, the accurate prediction of the SET-based upset is still an issue.

Monte Carlo simulation, as a complement to experimental tests, has become a necessary approach to evaluate the robustness of flip-flops in the design process [5–8]. Various Monte Carlo analysis tools or flows have been developed for SER analysis such as SEMM-2 [5] from IBM, MRED [6] from Vanderbilt University, and MUSCA SEP^3 [7] from ONERA. The conventional Monte Carlo evaluation approaches can manage to handle SEU caused by the direct upset [9]. However, evaluating SEU caused by the internal SET is still depended on other circuit simulation tools such as SPICE [10,11]. Because of the approximate transient current source model implemented in the circuit simulation, the conventional evaluation approaches can only obtain an approximate SEU prediction result. Therefore, improving the evaluation method for the SET-based upset will help to determine the overall SER of flip-flops more accurately.

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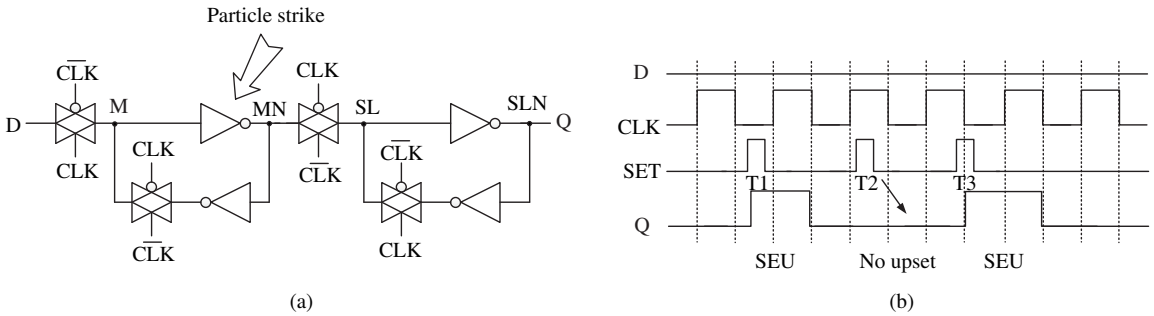

Figure 1 SEU caused by the direct upset and the SET-based upset. (a) The DFF is implemented in master-slave configuration. A SET is generated in the master stage when a particle strikes it; (b) timing chart of DFF with three different SET pulses.

In this paper, an improved Monte Carlo evaluation approach is proposed to evaluate SER for D flip-flops (DFFs). Compared with the conventional Monte Carlo evaluation approaches, the proposed evaluation approach adds two interaction segments. First, three-dimensional technology computer aided design (3D-TCAD) tool is performed to determine the relationship between the SET pulse width and the collected charge before evaluating SER for DFFs. Then, a novel SET-based upset model is based on 3D-TCAD results to predict SEU caused by the internal SET in Monte Carlo simulation. A DFF test chip was fabricated in a commercial 65 nm bulk process to validate the accuracy of the proposed evaluation approach.

2 SET-based upset mechanism in flip-flops

With the increase of the operating frequency, the internal SET induced upset becomes significant. This SET-based upset is similar to an SET that is generated in the combinational logic and subsequently latched in a flip-flop, except that the SET is generated inside the flip-flop itself [3]. Figure 1(a) shows the DFF configuration considered in this paper and Figure 1(b) shows three different SET pulses (T1–T3) generated in the D-latch master stage when an energetic particle strikes it. If the master stage is in latched state, a direct upset occurs and it would cause SEU at the output node Q (T1). While when the master stage is in transparent state, it may cause a SET-based upset.

The logic and the electrical maskings fail to mitigate the SET-based upset because the SET propagates through just a few gates in the latch cell [3]. Only the temporal masking affects the SET-based upset. If the SET pulse is far from the falling-edge of the operating clock, it would not be latched by the mater stage and an SET-based upset can hardly occur (T2). On the contrary, the SET pulse would cause an SET-based upset when it is near the falling-edge of the clock (T3). With the increase of the operating frequency, the SET pulse has a higher probability to be captured. Therefore, the SET-based upset would become a key issue to cause SEU in flip-flops at high operating frequency. Incidentally, improving the evaluation method for the SET-based upset is necessary.

3 The improved Monte Carlo evaluation approach

The conventional Monte Carlo evaluation approaches are not capable to handle the SET-based upset because they could not consider the temporal masking effect. They are depended on other circuit evaluation methods to determine the SET-based upset. The transient current source, such as the double-exponential current source, is used to model the transient current generated by the incident particles. Then the circuit response is simulated when the current source is injected in the circuit sensitive node. Due to the discrepancy between the real transient current and the current source, the circuit evaluation methods could only achieve an approximate SEU prediction result caused by the internal SET [10]. Furthermore, different layout structures, such as the well configuration and the transistors density, significantly influence the

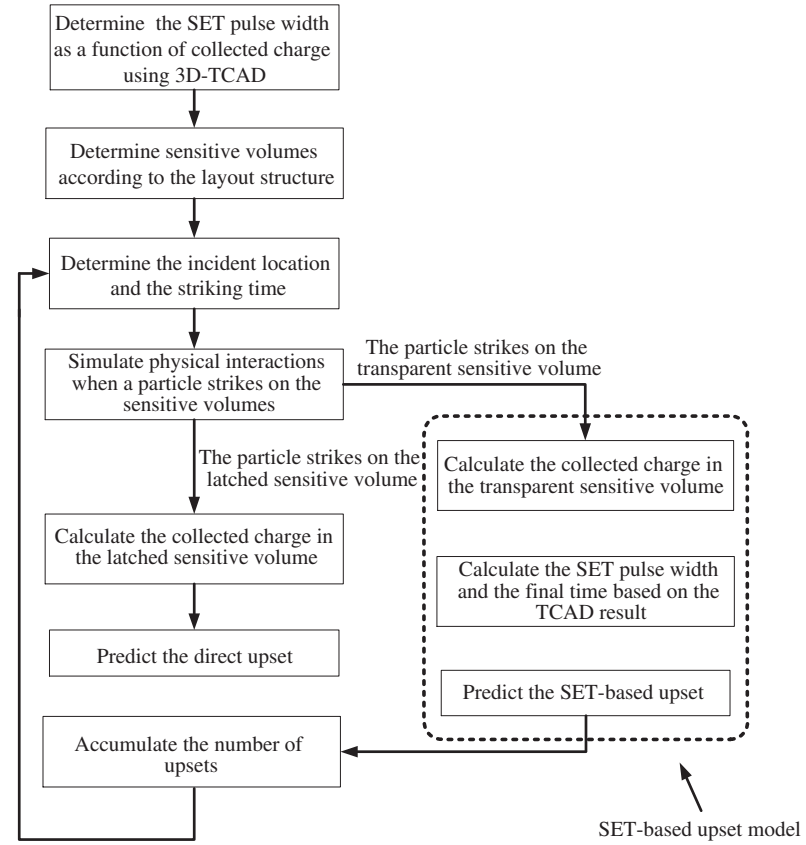

Figure 2 Process to implement the improved Monte Carlo evaluation approach.

shape of the transient current [12,13]. It increases the discrepancy between the real transient current and the current source implemented in the circuit simulation.

To substitute the circuit evaluation methods, the improved Monte Carlo evaluation approach adds two interaction segments. The first segment aims to establish a look-up table of the relationship between the SET pulse width and the collected charge. This look-up table is obtained by 3D-TCAD simulation. The other segment contains a SET-based upset model. This model is implemented in Monte Carlo simulation to calculate SET pulse width and to determine the SET-based upset. The proposed SET-based upset model makes the Monte Carlo evaluation approach capable to handle SEU induced by the internal SET. Figure 2 shows the process to implement the improved Monte Carlo evaluation approach. The dashed segment is the proposed SET-based upset model which is responsible for predicting SEU caused by the internal SET. The other segment is performed to predict SEU caused by the direct upset, which is similar to that of the conventional Monte Carlo evaluation approach.

3.1 Determining the SET-charge relationship

Before evaluating SER of DFFs, 3D-TCAD tool is performed to determine the relationship between the SET pulse width and the collected charge in each sensitive node. 3D-TCAD tool has been proved to be useful in investigating the physical mechanism of single event effects [14–16]. Therefore, using 3D-TCAD tool can obtain an accurate SET-charge relationship. Based on 3D-TCAD results, the SET-based upset model is able to calculate the SET pulse width and predict the SEU induced by the internal SET. Furthermore, this three-dimensional device analysis tool can take into account the technological parameters and the layout structure. Employing different technological process or different layout structures, it could obtain a different SET-charge relationship.

In this paper, based on the commercial 65 nm bulk process and the DFF layout structure shown in Figure 3, we use Sentaurus TCAD tool to obtain the relationship between the SET pulse width and

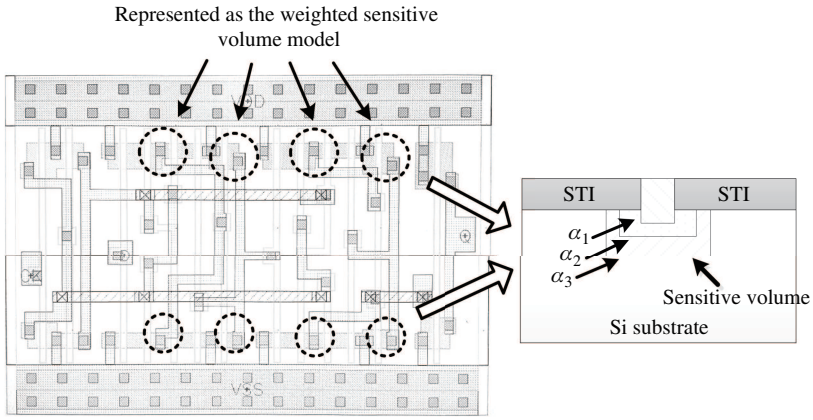

Figure 3 GDS view of the DFF in 65 nm bulk process. All sensitive nodes are represented by the weighted volume model.

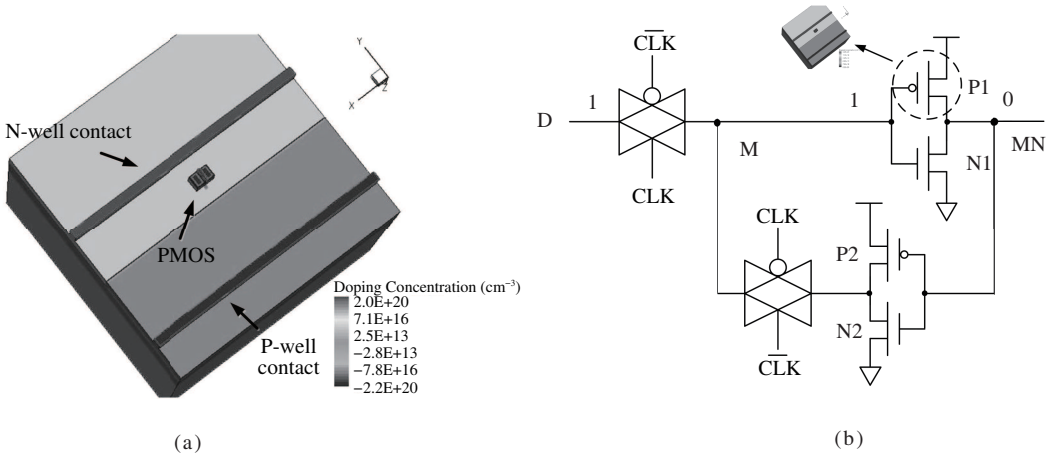

Figure 4 The simulation circuit in 3D-TCAD. (a) The PMOS transistor scheme for TCAD simulation; (b) the sensitive transistor P1 is represented as TCAD scheme and the other transistors are represented as the corresponding SPICE model.

the collected charge in each sensitive node of DFFs. Figure 4(a) shows the PMOS transistor scheme for TCAD simulation. The NMOS transistor has a similar scheme. The PMOS transistor is calibrated to match the DC and AC electrical characteristics (e.g. $I_{\rm ds}$-$V_{\rm ds}$ and $I_{\rm ds}$-$V_{\rm gs}$ curves) based on the commercial 65 nm PDK. The sensitive transistors are simulated as the TCAD scheme, and the other transistors are modelled corresponding to their SPICE model. For example, when the input data and the clock signal are HIGH, transistor P1 is susceptible to radiation. Therefore, transistor P1 is modeled as TCAD scheme and other transistors are modeled as corresponding SPICE models, as shown in Figure 4(b). Then 3D-TCAD tool simulate single-event effect when heavy ions strike transistor P1. The collected charge and SET pulse width are calculated with different LET, and the SET-charge relationship in sensitive node MN is determined subsequently. Similar approaches are carried out to determine SET-charge relationship in other sensitive node.

Physical models used in TCAD simulation included Fermi-Dirac statistics, band-gap narrowing effect, Auger recombination, and doping dependent, electric field dependent, and carrier-carrier scattering mobility models. Unless otherwise specified, the default models and parameters provided by Sentaurus TCAD vH-2013.03 are used here.

Figure 5(a) shows the SET-charge relationship in the sensitive node M and MN. We can observe that the SET pulse width is nearly linear relation of the collected charge. In our previous works, The SET pulse width generated by an individual particle event is nearly linear with linear energy transfer (LET) in the sensitive node [17,18]. When incident particles strike at normal incidence, the particle tracks in the

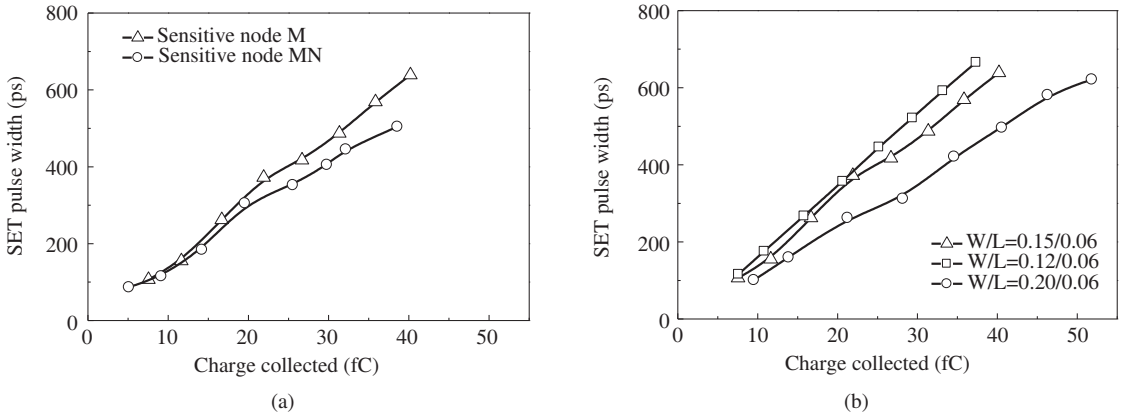

Figure 5 The SET pulse width as the function of the charge collected in (a) the sensitive nodes M and MN; (b) the SET-charge relationship with different dimensions of the on-state transistor N1.

sensitive volume are approximate consistent with different LET particles. Hence the energy deposited and charges collected in the sensitive volume are linear with LET, and it shows a liner relationship with the SET pulse width. The same trend is also observed in the sensitive nodes of the slave stage.

Moreover, some layout factors or operation conditions are significant influence on the SET-charge relationship. For example, Figure 5(b) shows the SET-charge relationship in sensitive node MN with different dimensions of the on-state transistor N1. A higher W/L ratio increases the NMOS drive current. It will mitigate the SET characteristics in the sensitive node MN. Therefore, we can observe a different SET-charge relationship with the width of transistor N1 increases. To obtain an all-around look-up table of SET-charge relationship, we use 3D-TCAD tool to simulate single-event effect with different transistor dimensions, well configurations, temperature and supply voltage. The look-up table can generate an accurate SET-charge relationship with different layout structures and different operation conditions.

3.2 The SET-based upset model

After determining the SET-charge relationship, the proposed SET-based upset model is implemented to determine the SET-based upset in Monte Carlo simulation. First, all the sensitive transistors in the DFF circuit are represented as the sensitive volumes V_i during Monte Carlo simulation. Then, an one-dimensional random function obeying uniform distribution is used to model a random strike time T_0. A two-dimensional random function is performed to determine incident locations before each particle strike. According to the striking time, the state (transparent or latched) of each sensitive volume V_i in DFFs can be determined. Assuming that an incident particle strikes the DFF circuit when the clock signal is HIGH, the sensitive volumes in master stage are transparent and the sensitive volumes in slave stage are latched. Only the transparent state of sensitive volumes would cause an SET-based upset. The latched state of sensitive volumes would cause a direct upset.

Then Monte Carlo tools simulate particles to strike the DFF circuit. The deposited energy E_i and the collected charge C_i in each sensitive volume V_i are calculated. If the state of the sensitive volume is latched, SEU caused by the direct upset is predicted to occur when the calculated charge exceeds the critical charge. If the state of the sensitive volume is transparent, based on the layout structure and operation conditions, the proposed SET-based upset model chooses an appropriate SET-charge relationship to calculate the SET pulse width.

The final time T_{final} is the summation of the strike time T_0 and the SET pulse width. If the initial time T_0 is less than the half period while the final time exceeds it, or the initial time T_0 exceeds the half period and the final time exceeds the full period; SEU caused by the internal SET is predicted to occur. On the contrary, the SET pulse is not latched and an SET-based upset can hardly occur. Consequently, the proposed SET-based upset model is able to predict SEU caused by the internal SET instead of the circuit evaluation methods. Because it is based on 3D-TCAD results to calculate the SET pulse width,

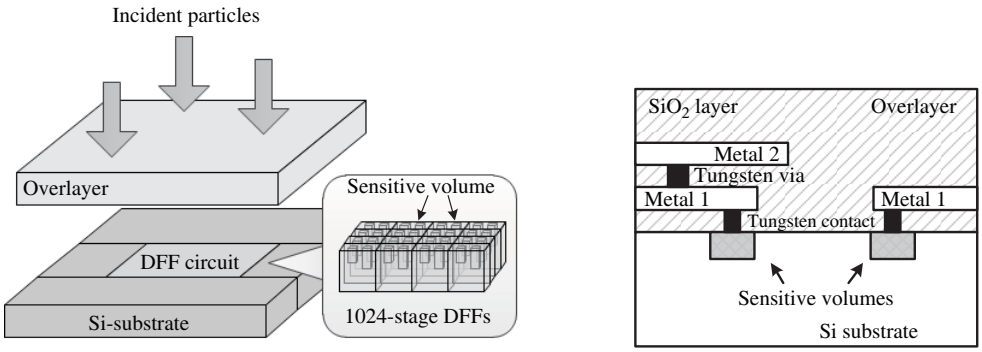

Figure 6 The simulation structures implemented in Monte Carlo simulation. (a) The 3D configuration of the simulation structure; (b) the 2D section of the simulation structure.

the SET-based upset model would predict SEU caused by the internal SET more accuracy than the circuit evaluation methods.

In conclusion, the proposed evaluation approach is capable to handle SEU caused by both the direct upset and the SET-based upset in Monte Carlo simulation. Since the SET-based upset model is able to predict SEU caused by the internal SET accurately, the proposed evaluation approach improves the overall SER evaluation accuracy compared with the conventional Monte Carlo evaluation approaches. Furthermore, the time cost for the proposed evaluation approach is just a slight higher than the conventional evaluation approaches because the proposed evaluation approach only adds a SET-based upset model in Monte Carlo simulation.

3.3 Simulation setup

The Monte Carlo simulation tool Geant4.9.5 is used to simulate the energy deposited and charge collected in the sensitive volumes. All sensitive active areas in the DFF layout are represented as sensitive volumes, as shown in Figure 3. The weighted sensitive volume model which is proposed in [19] is used to calculate the collected charge in each sensitive volume. This model contains several nested volumes. The following equation relates energy deposited in the sensitive volume to the charge collected on the corresponding circuit node. It quantifies the charge collection at a sensitive node as a linear combination of the energy deposited in each volume scaled by the respective collection efficiency coefficient α_i which is calibrated by 3D-TCAD tool.

$$Q_{\text{collect}} = \frac{1 \text{ pc}}{22.5 \text{ Mev}} \sum_{1}^{N} \alpha_i \times E_{\text{depi}}. \tag{1}$$

The simulation configuration implemented in Monte Carlo simulation is shown in Figure 6(a). The DFF circuit consists of 1024-stage DFFs. The overlayer which is obtained from the device manufacturer is also considered in Monte Carlo simulation. It contains the Al metallization layer, the SiO_2 passivation layer and the tungsten via, as shown in Figure 6(b). The dimension and location of the metallization layer and the tungsten via are based on the DFF layout structure. The following prepackaged physical processes in Geant4 are used during Monte Carlo simulation: ionization, nuclear elastic and inelastic reactions, and coulombic scattering.

4 Experiment validation

4.1 Experiment setup

To validate the accuracy of the improved Monte Carlo evaluation approach, a DFF test chip was fabricated by the commercial 65 nm bulk Complementary Metal Oxide Semiconductor (CMOS) process. The

Table 1 Heavy ions used in the experiment

Ion	Energy at the Silicon Surface (MeV)	Effective LET (MeV·cm^2/mg)	Range (μm)
S	165	11.3	51.8
Ti	185	21.2	37.9
Br	250	40.2	35.5
I	295	64.4	30.8

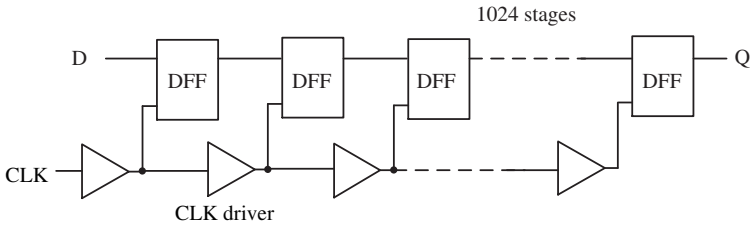

Figure 7 The schematic diagram of the test circuit containing a 1024-stage shift register chain.

schematic diagram of the DFF is shown in Figure 1(a) and the layout structure is shown in Figure 3. The test circuit contains a 1024-stage shift register chain, as shown in Figure 7. All the signal (D, Q and CLK) pins of the test circuit are connected to the FPGA. Error detection was implemented by FPGA and the error counts were exported to the computer by serial interface. Heavy ion experiment was conducted at the HI-13 Tandem Accelerator in China Institute of Atomic Energy using the ion beam at normal incidence on the test element. The characteristics of the four ions used in the test are listed in Table 1. The incident ion dose rate is 1×10^4 ions/cm$^2 \cdot$s and the fluence of each incident ions is 1×10^7 ions/cm^2.

The SEU cross-sections were measured with nominal VDD of 1.0 V at room temperature in two different test modes. In the static test mode, all 0 data pattern (S00) or all 1 data pattern (S11) was first loaded into the shift register chain. The device was then exposed to heavy ions and the stored data were read out and compared to the original one after irradiation. During the irradiation, the clock signal CLK was held either at a constant HIGH value or a constant LOW value. The constant CLK signal ensures that the internal SET caused by ions could not be propagated and latched during irradiation. Hence the static test mode can eliminate SEU caused by the internal SET.

In dynamic test mode, the test circuit was irradiated with dynamic 0 (D00) data pattern or dynamic 1 (D11) data pattern. Since the data pattern is fixed to a constant LOW value or a constant HIGH value, it can avoid the soft errors caused by the clock tree. The upset in clock tree may cause the data shifted forward without any error. In this test mode, both the direct upset and the SET-based upset could cause soft errors. Once one stage of the shift register chain is corrupted by the heavy ion, the subsequent ones in the chain will propagate the upset value until it is read by the FPGA. Dynamic test mode was conducted with operating frequencies range from 2.5 MHz to 160 MHz to investigate the frequency dependency.

4.2 Comparison of simulation and experimental results

The improved Monte Carlo evaluation method is implemented to predict soft errors of the test circuit. The number of each incident ion is 1.58×10^4 which is calculated by multiplying the ion fluence and the test chip area. The incident ion amount makes sure the ion fluence in Monte Carlo simulation is consistent with the experimental conditions.

The statistical upset amount in heavy ion experiment and Monte Carlo simulation are presented in Tables 2 and 3. The SEU cross-sections are shown in Figures 8 and 9. The cross-section is defined as the total number of SEUs captured in each heavy ion radiation divided by the fluence (1×10^7 ions/cm^2) and the stages of the shift register chain (1024). Table 2 and Figure 8 show the discrepancy of the statistical upset amount and the cross-section between the static test mode and the 160 MHz dynamic test mode. The SET-based upset shows a significant effect on soft errors in the experimental results.

Table 2 The statistical upset amount with different test modes

LET	S00 static test mode		D00 dynamic test mode		S11 static test mode		D11 dynamic test mode	
	Exp.	Sim.	Exp.	Sim.	Exp.	Sim.	Exp.	Sim.
11.3	135	117	617	545	119	117	546	545
21.2	375	353	889	984	212	261	819	984
40.2	445	521	1125	1349	272	337	929	1349
64.4	441	481	1455	1446	298	420	1177	1446

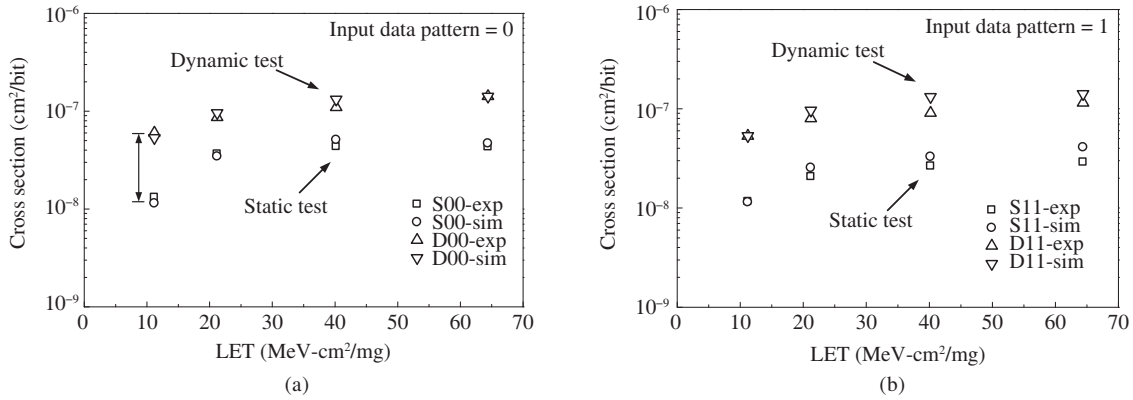

Figure 8 SEU cross-sections calculated by Monte Carlo simulation and heavy ion experiment. The cross-section versus LET in the static test mode and the 160 MHz dynamic test mode. (a) The input data pattern is "0"; (b) the input data pattern is "1".

The cross-sections in the dynamic test mode have approximate one order of magnitudes higher than the cross-sections in the static test mode. The direct upset is independent of the operating frequency and the increased upsets in dynamic test mode are mainly due to the SET-based upset. Therefore, in order to evaluate the overall SER of DFFs accurately, it should improve the SEU prediction method caused by the internal SET.

The improved Monte Carlo evaluation approach we proposed shows consistent in both the static test and the 160 MHz dynamic test modes. The average difference between experiments and simulations is close to 10% in both the static test mode and the 160 MHz dynamic test mode. These simulation results indicate that the proposed Monte Carlo evaluation approach is capable to accurately predict SEU caused by both the direct upset and the SET-based upset.

The frequency dependency in the dynamic test mode is illustrated by Table 3 and Figure 9. The experimental cross-section shows a slight increase with the increase of the operating frequency. The statistical upset amount in the high operating frequency is about 1.2X higher than that in the low operation frequency. This trend is consistent with the data in reference [3]. The same trend is also observed in Monte Carlo simulation results. When the operating frequency is below 10 MHz, the simulation result shows a little discrepancy compared with the experimental result. The maximum difference between experiments and simulations is about 26.46% and 11.25%, respectively. With the increase of the operating frequency, it shows more accuracy.

5 Discussion

5.1 Compared with the conventional evaluation approach

In order to investigate the improvement of the proposed Monte Carlo evaluation approach, we also use the conventional evaluation approach described in [10,11] to evaluate SER of DFFs. Monte Carlo simulation is performed to model the energy deposited and charge collected in the sensitive transistors.

Table 3 The statistical upset amount with different operating frequencies

Frequency	LET = 11.3 MeV-cm^2/mg		LET = 40.2 MeV-cm^2/mg	
(MeV)	Exp.	Sim.	Exp.	Sim.
2.5	443	348	979	720
10	498	360	1082	769
40	584	418	1119	977
160	617	545	1125	1349

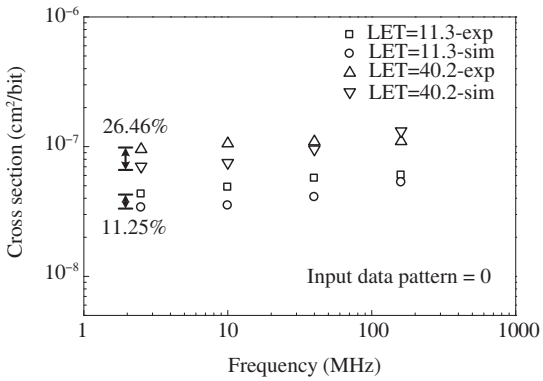

Figure 9 SEU cross-sections calculated by Monte Carlo simulation and heavy ions experiment. The input data pattern is 0 and the cross-section versus the operating frequency.

Table 4 Comparison of the two evaluation approaches in the static test mode

LET	The proposed evaluation approach		The conventional evaluation approach	
	Simulated cross-section	Relative errors (%)	Simulated cross-section	Relative errors (%)
11.3	1.14×10^{-8}	13.63	1.21×10^{-8}	8.33
21.2	3.44×10^{-8}	6.01	3.62×10^{-8}	10.91
40.2	5.08×10^{-8}	9.78	4.96×10^{-8}	11.29
64.4	4.69×10^{-8}	8.81	4.71×10^{-8}	9.52

Then double-exponential current source described in [11] is implemented in SPICE circuit simulation for circuit response and predict SEU. This current source is widely used for modeling the transient current generated by the incident particles. The following expression is used to calculate the SPICE transient current:

$$I(t)=\begin{cases}0, & t<t_{d1},\\ I_m\left(1-\exp\left(\frac{-(t-t_{d1})}{\tau_1}\right)\right), & t_{d1}<t<t_{d2},\\ I_m\left(\exp\left(\frac{-(t-t_{d2})}{\tau_2}\right)-\exp\left(\frac{-(t-t_{d1})}{\tau_1}\right)\right), & t>t_{d2},\end{cases} \tag{2}$$

where t is time, t_{d1} is the onset of the rise of the current, t_{d2} is the onset of the fall of the current, I_m is the saturation current of the complementary on-state transistors, τ_1 is the rise time constant, and τ_2 is the fall time constant. The integral of the transient current over time must be equal to the total collected charge in Monte Carlo simulation. The calculated transient current is injected into the sensitive node of the test circuit and the circuit response is simulated by SPICE simulation tool. The injection number, location and time are consistent with Monte Carlo simulation. The input data pattern is fixed to a constant LOW value. The time for rise and fall are set to 10 ps and 20 ps, which are determined by 3D-TCAD simulation.

The simulation results of the proposed Monte Carlo evaluation approach and the conventional evaluation approach in the static test mode is shown in Table 4. Both the proposed Monte Carlo evaluation approach and the conventional one can accurately predict SER of DFFs compared with the experimental

Table 5 Comparison of the two evaluation approaches in the 160MHz dynamic test mode

LET	The proposed evaluation approach		The conventional evaluation approach	
	Simulated cross-section	Relative errors (%)	Simulated cross-section	Relative errors (%)
11.3	5.68×10^{-8}	6.77	2.74×10^{-8}	48.50
21.2	1.07×10^{-7}	11.46	5.68×10^{-8}	40.83
40.2	1.45×10^{-7}	10.68	8.20×10^{-8}	37.13
64.4	1.58×10^{-7}	12.06	8.98×10^{-8}	36.31

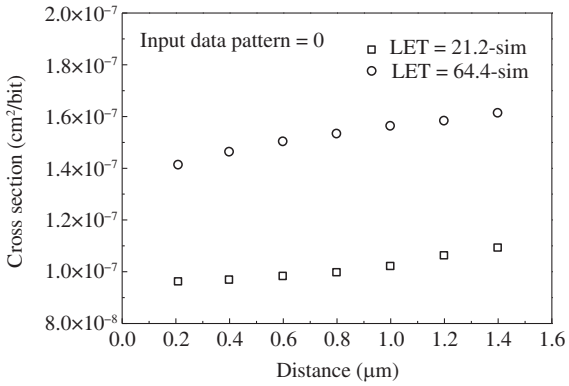

Figure 10 The simulation cross-section of the proposed evaluation approach when the distance between the well contact and the transistors increases.

data. The difference between experiments and simulations is only about 10% in these two evaluation approaches. In the static test mode, the internal SET pulse would not be propagated and are latched during irradiation. SEU is only caused by the direct upset. Therefore, the two evaluation approaches have the same prediction accuracy in the static test mode.

Table 5 shows the simulation results of the two evaluation approach in the 160 MHz dynamic test mode. We can observe that the simulation results of the proposed Monte Carlo evaluation approach still have about 10% relative errors compared with the experiment data. However, the simulation results of the conventional evaluation approach shows a large discrepancy. In the 160 MHz dynamic test mode, the SET-based upset has become significant. The large discrepancy indicates that the circuit evaluation method used the transient current source could only obtain an approximate SET-based upset prediction results. Therefore, the overall SER prediction result by the conventional evaluation approach shows a large discrepancy compared with the experiment data.

Instead of the circuit evaluation method, the proposed Monte Carlo evaluation approach adopts the SET-charge relationship to calculate the SET pulse width generated at the sensitive node. This calculation method does not use the imprecise transient current model to determine the SET pulse width. Therefore, the proposed Monte Carlo evaluation approach has more accuracy than the conventional evaluation approach in the dynamic test mode.

5.2 Effect of the layout structure

In our previous works, we reported that different layout structures had significant influence on the SET pulse generated by the incident particles [12]. For example, the SET pulse width increases with the increase in space between the well contact and the transistors. The increased SET pulse has a higher probability to be captured and the SET-based upset would become easier to occur. Therefore, different layout structures would have significant influence on the overall SER of DFFs in the dynamic test mode.

However, the circuit simulation in the conventional evaluation approach could not take the layout structure into consideration. It would get a similar SER prediction result when the layout structure is changed. The evaluation approach we proposed is able to consider the change of the layout structure. 3D-TCAD tool could get a different SET-charge relationship according to the different layout. Hence the

proposed evaluation approach could obtain the SET pulse width by the different SET-charge relationship. Figure 10 shows the simulation results of the proposed evaluation approach in 160 MHz dynamic test mode when the space between the well contact and the transistors increases. It can be observed that the simulated cross-section has a slight increase with the increasing distance.

6 Conclusion

The internal SET induced upset in flip-flops has become significant with the increase of the operating frequency. The accurate prediction of SEU caused by the internal SET is still an issue in the conventional SER evaluation approaches. In this paper, an improved Monte Carlo evaluation approach is proposed to predict SER of DFFs. 3D-TCAD tool is performed to determine the relationship between the SET pulse width and the collected charge according to the layout structure. Based on 3D-TCAD results, a novel SET-based upset model is performed to predict SEU caused by the internal SET in Monte Carlo simulation.

The proposed Monte Carlo evaluation approach can handle SEU caused by both the direct upset and the SET-based upset. It does not depend on the circuit evaluation method to predict SEU caused by the internal SET. Therefore, the proposed evaluation approach improves the overall SER evaluation accuracy when compared with the conventional Monte Carlo evaluation approaches. Moreover, the layout structure is also taken into account in the proposed Monte Carlo evaluation approach which obtains a different SER prediction result as per the layout structure.

Heavy ion experimental results are used to validate the accuracy of the proposed Monte Carlo evaluation approach. Simulation results are consistent with the experimental results in both the static test mode and the 160 MHz dynamic test mode. Frequency dependence is also investigated in this paper. The proposed Monte Carlo evaluation approach shows the same trend compared with the experimental data. It has more accuracy with the increase of the operating frequency.

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