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A low-power, area-efficient all-digital delay-locked loop for DDR3 SDRAM controller

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Abstract A new low-power, area efficiency all-digital delay-locked loop (ADDLL) circuit is proposed for DDR3 application. The ADDLL can process the input clock frequency ranging from 333 MHz to 800 MHz (DDR3-667/800/1066/1600) by using Phase Detector (PD), Delay Control Delay Line (DCDL), Digital Loop Filter Controller (DLFC) and Delay Generator (DG). To achieve 1.6 Gb/s/pin operation, a novel DCDL scheme is employed. The DCDL has a small delay with a shunt capacitor based digitally controlled delay element. A split-control thermometer-code generator generates the control voltages used to set a current in the current-starved inverters. The testchip fabricated with a 40-nm CMOS process gives the ADDLL data rate of 667 Mbps–1.6 Gbps. Experimental results that show the power consumption is 1.87 mW at 1.1 V with active area is 0.0137 mm^2.

Keywords all-digital delay-locked loop, double-data-rate, digitally controlled delay line, shunt capacitor, thermometer code

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1 Introduction

Delay-locked loop (DLL) and Phase-locked loop (PLL) are commonly used to solve the clock synchronization problem. However, the DLL is more suitable for the clock de-skew problem than PLL due to the simple design architecture. Moreover, the DLL also provides better jitter performance considering that there is no jitter accumulation in a voltage controlled delay line (VCDL) or digitally controlled delay line (DCDL). The application of DLL is not only limited to the clock synchronous but it is also useful for Double-Data-Rate Three (DDR3) SDRAM [1–4]. The advantages of an all-analog DLL are low jitter output and higher delay resolution. In [5], an all-analog DLL improves the locking range by using replica delay line. The disadvantage is lower noise immunity and a longer design cycle. An all-analog DLL is not suitable for the process portability and poor noise immunity. Therefore, digital DLL is developed to address these problems [3,4]. Digital DLL can get the extra advantages of less silicon area and deliver GDSII database quickly in around 3 weeks.

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As the need for high performance communication system is increasing, the progressive use of low power and high speed memory technology becomes more important. DDR3 SDRAM can be one of the good storage solutions owing to its low voltage and high speed operation. For the high speed up to 1600 MT/s DDR3 SDRAM, the maximum additive latency (AL) of 0 and CAS write latency (CWL) of 8 should be supported. The DLL circuit is used as a clock generator to adjust the output data timing with the input clock. The DLL for DDR3 SDRAMs must have an operating range from 333 to 800 MHz at 1.1 V core voltage. In this paper, a low jitter DLL with a novel DCDL scheme using shunt capacitor generating a required number of delaysa DLFC circuit replace charge pump and capacitor to reduce bias current in charge pump to save current consumptionand current-starved schemes are proposed for high frequency operation.

The proposed all-digital DLL circuit generates one-channel DQS with the fixed timing delays to be used by the DDR3 SDRAM controller. This ADDLL integrates a PD using D flip-flops that detects the phase lag or phase lead between the reference input clock (333–800 MHz) signal FREF and the Output clock range signal CKOUT, and generates the UP/DOWN output signals for phase adjustment. The DLFC circuit generates digital signals to control the amount of the delay time in the DCDL and delay generator. If CKOUT signal leads CKIN signal, the DLFC circuit adjusts the digital signals to increase the delay time in the DCDL. The DCDL circuit uses the control code output by the DLFC circuit to control current-starved delay cell and generates the required number of delay by shunt capacitor. The delay generator is duplicated 1/4 delay cells utilized in the DCDL circuit to generate an overall 25% phase delay. The ADDLL supports an operating voltage ranging from 0.99 to 1.21 V with an operating junction temperature ranging between −40°C and 125°C. The ADDLL circuit can process the input clock frequency ranging from 333 to 800 MHz (DDR3-667/800/1066/1600). This DLL can be used by the DDR3 SDRAM controller to generate a delay of 25% of the FREF period for the DQS signal during the DQ data latch process.

The rest of this paper is organized as follows. Section 2 presents the architecture of the proposed ADDLL. Later, the design concepts of the main building blocks in DCDL are introduced individually. Section 3 shows the experimental results. Conclusions are given in Section 4.

2 Circuit description

2.1 Architecture of phase-shift DLL

Figure 1 shows the block diagram of the proposed ADDLL. The DLL consists of two control loops, one is the delay control loop and the other is the duty cycle control loop. The delay control loop consists of a bang-bang PD based on three states D flip-flops, a DLFC that is based on an up-down counter substitutes for the shift register to control the delay line [6] with successive approximation register (SAR) [7] that uses binary search manner and the Main Delay Line. The locking time is an important parameter for digital DLL to evaluate the performance, especially in high-speed memory applications. An improved SAR DLL [8] was proposed to resolve this problem by using the counter-controlled control word instead of SAR-controlled.

The duty cycle control loop consists of the DCDL and the Main Delay Line. DCDL is the key component of ADDLL. Like most voltage controlled delay line (VCDL), the DCDL consists of several different digitally controlled delay elements (DCDE). There are two main parameters to adjust the delay time of DCDL. One is the total number of the delay elements, usually taken for the coarse tune method, and the other is the propagation delay time of the delay elements (i.e. inverters), which is usually taken for the fine tune method.

2.2 Digitally-controlled delay line (DCDL)

Among the functional blocks of all-digital clock generators, digitally controlled oscillator (DCO) is the kernel module, for the reason that it dominates overall performance including power consumption of

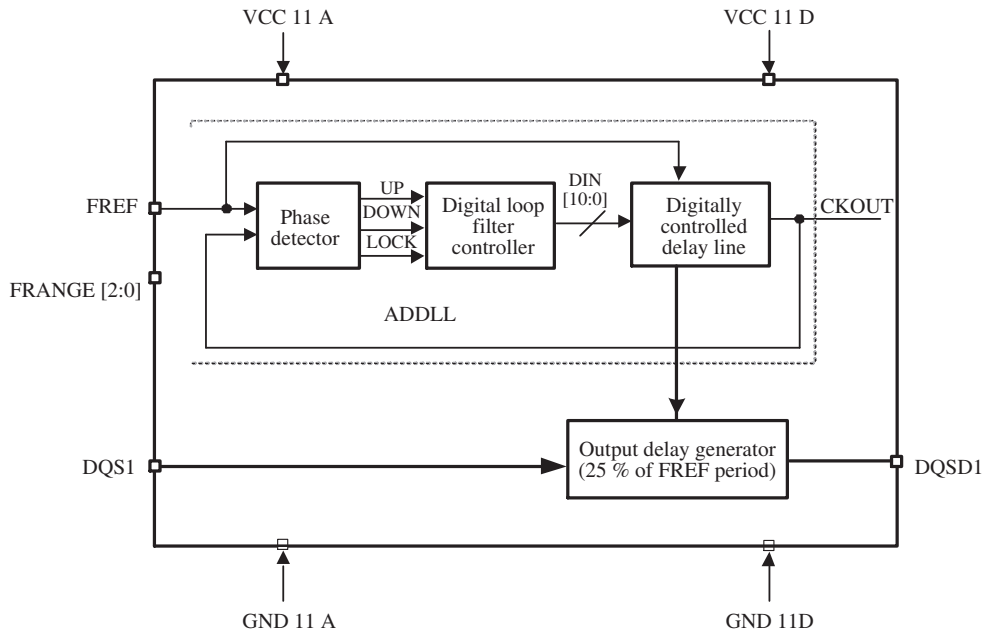

Figure 1 Block diagram of the proposed ADDLL.

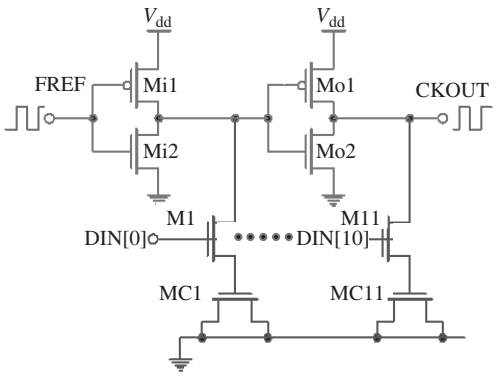

Figure 2 Shunt capacitor based digitally controlled scheme.

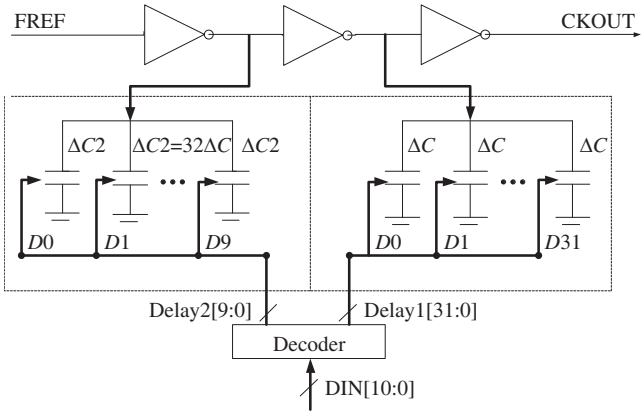

Figure 3 Schematic of digitally controlled decoder with shunt capacitor.

all-digital clock generator. For example, DCO exceeds 50% power consumption of all-digital clock generator [9], and the delay resolution, operating range affect jitter performance and output frequency range of all-digital clock generator. The LC tank based DCO architecture for RF frequency synthesizer, which can achieve high delay resolution was reported in [10]. Two effective solutions have been proposed to design a high resolution DCO. First solution improves driving strength in the MOS using a fixed loading capacitor and achieves a high resolution [11]. The latter solution uses a new technique for the optimal shunt capacitor to fine tune the loading capacitance and obtains high resolution [12]. Figure 2 shows a scheme for using a shunt capacitor based DCDE [13]. In this circuit, MC1–MC11 acts as shunt capacitors. The gate of transistor M1–M11 controls the discharging and charging current to the MC1–MC11 capacitors. Therefore, control bit DIN [n] can control the delay resolution from FREF to CKOUT. The delay time of inverter circuit by using a shunt capacitor method can be controlled in binary-weight to meet the delay time requirement.

Figure 3 illustrates the schematic diagram of the proposed digital control decoder (DCD) with 8 bits binary weighted control [14]. The DCD is used to control the capacitance values of the conductive capacitor by the output signal from the DLFC circuit. The tuning stage is divided into Delay1 and Delay2 stages to increase the resolution of the decoder. The capacitance values depend on the requirement of

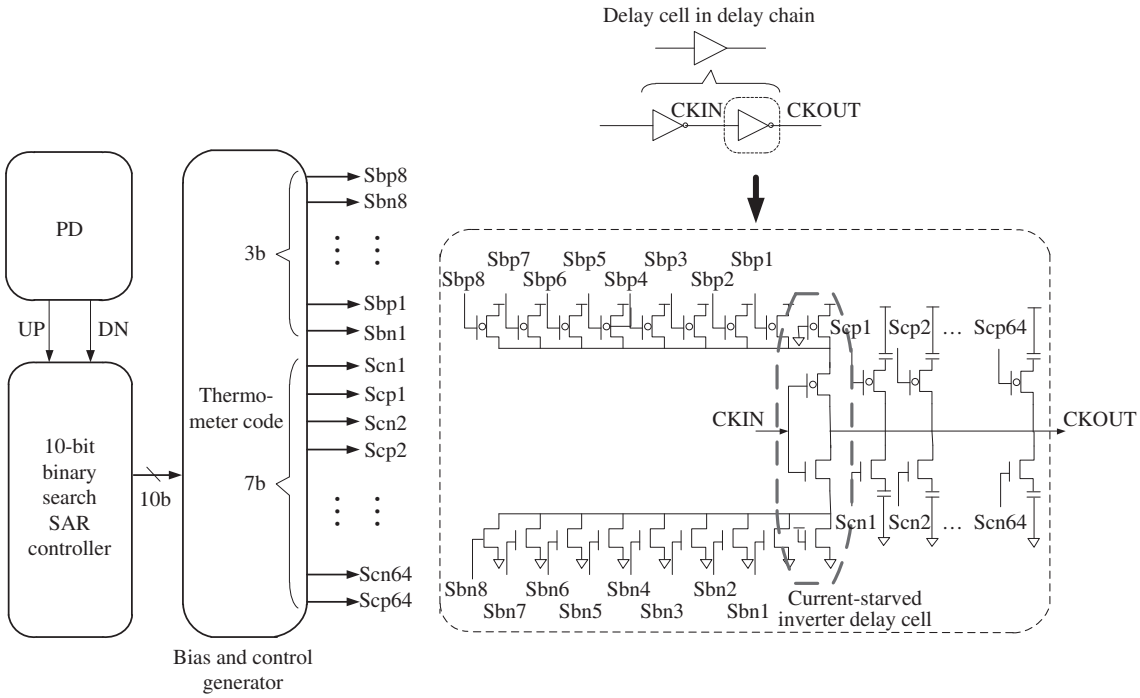

Figure 4 Schematic of delay cell with bias voltage.

resolution. The Delay1 stage consists of 32 shunt capacitors with capacitance difference of C. 32 uniform C are used to make single $C2$ shunt capacitors. The total capacitance difference is equal to 352 C shunt capacitance. The proposed DCD with shunt capacitor can enhance delay resolution by 352 times compared to that of a simple buffer amplifier.

To meet requirements of the frequency range of DDR3 SDRAM specification, a current-starved inverter is used to replace the simple inverter in the output stage [15]. A traditional CMOS inverter in the center and two transistors along top and bottom surfaces serve as adjustable current supplies with both pMOSFET tail sourcing current and nMOSFET tail sinking current. The nMOSFET and pMOSFET act as current sources to set the current conduction level. Figure 4 shows a schematic diagram of the delay cell in delay chain circuit. DCDL is composed of eight identical current-starved delay cells. Eight delay cells used in the delay line lock one cycle of delay to the target frequency. The output delay generator shown in Figure 1 generates a 90° delay by two delay cells. The cascade of eight current-starved inverters consists of eight separate transistors in each stage, controlled by a bias voltage of the delay chain. The operating frequency range is determined by the transistor. Eight frequency bands from 150 to 800 MHz are controlled by three control bits FRANGE [2 : 0].

128 capacitors are connected close to the output node to adjust further quantization into delay value. In total 1024 delay units can be adjusted through eight delay cells and 128 capacitors in each cell. The control circuit of the thermometer-code generator is to generate the control voltages used to set a current in the current-starved inverters. The bias voltages are generated by eight 10-bit thermometer-code instead of binary-weighted DAC at each delay cell. The 10-bit digital control input signals of the thermometer-code generator generated by DLFC circuit adjusts the delay of the current-starved inverter based on delay line. Bias voltages Sbn1 to Sbn8 for nMOSFET transistors are controlled by three bits, and Sbp1 to Sbp8 for pMOSFET by current mirroring counterparts to keep the total delay time at the desired value. The 128 bias voltages (from Scn1, Scn2, to Scp64, Scp64) for capacitance load are generated by separated seven bit in thermometer-code generator. This split-control scheme makes the adjustment of low supply voltage delay elements in the desired operating range possible. This scheme also grants for lower power consumption and a smaller silicon area for an ADDLL.

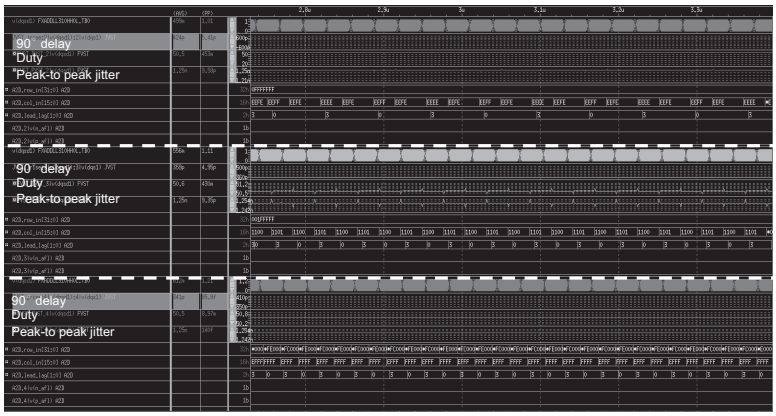

Figure 5 Simulation waveforms at three process corners.

3 Simulation and experimental results

3.1 Post-layout simulation results under three conditions

The proposed ADDLL is designed by using 40-nm CMOS cell library. After synthesis and APR, the netlist is simulated by using NCverilog. The closed-loop pre-layout simulation waveforms of entire circuit at 800 Mhz are shown in Figure 5. They correspond to three primary process corners (SSHTLV, TT, FFLTHV), respectively. After locking, the 90° delay values between DQS1 and DQSD1 are 424, 359, 341 ps under SSHTLV, TT, FFLTHV conditions, respectively. Compared to the theoretical value of 312.5 ps for the 90° delay at 800 MHz (FREF), the extra delay values are shifted by mux and bandgap circuits. The extra delay can be compensated by DDR3 PHY layer IP. On subtracting the intrinsic delay values (115, 46, 25 ps) in DDR3 PHY layer IP, the actual 90° delay values between DQS1 and DQSD1 are 309, 313, 316 ps under SSHTLV, TT and FFLTHV conditions, respectively. These performance values are close to the theoretical value of 312.5 ps.

3.2 Measurement setup

To verify the validity of the proposed ADDLL, a DUT test board was designed integrating the sample chip, pulse data generator, digital multimeter, DC power supply voltage and DSO Oscilloscopes. Figure 6 shows the experimental set up used to measure the performance of the ADDLL proposed in this paper. An operating frequency ranging from 333 to 800 MHz input in the DUT is offered by a pulse data generator. The Instek DC Power Supply PST-3201 provides high quality 1.1 V output voltages to the analog power (VCC11A) and digital power (VCC11D) pins on DUT that was packaged in TQFP-100. The jitters of the 2-channel input and output were measured at an analog power supply (VCCA) ranging from 0.99 to 1.21 V as the temperature swept from −40°C, 0°C, 25°C, 85°C, to 125°C. The power consumption is 1.87 mW at 800 MHz (FREF) with supply voltage of 1.1 V (both VCC11A and VCC111D).

3.3 Experimental results and analysis

Figure 7 shows the layout and microphotograph of the proposed ADDLL chip. The local DLFC circuit is implemented through logic synthesis and auto placement and routing (APR). The other modules are implemented by the customized design to improve the performance and meet the 800 MHz requirement. The circuit was implemented using the 40-nm CMOS process with an area of 111 μm × 80 μm.

Figure 8 shows that the measured results of the phase shift errors vary from output clock at 800 MHz. Six samples labeled as T1, T2, S2, S4, F2, F5 are measured at 25°C. The shift errors variation is plotted on a graph of different process where voltage (x-axis) versus delay time (y-axis). Delay time of maximum specification is 477 ps (362 ps + 115 ps) and minimum is 288 ps (262 ps + 26 ps). The ideal delay time from DQS to DQSD is 368.5 ps (312.5 ps + 56 ps). Therefore, the phase shift errors of sample T1 with

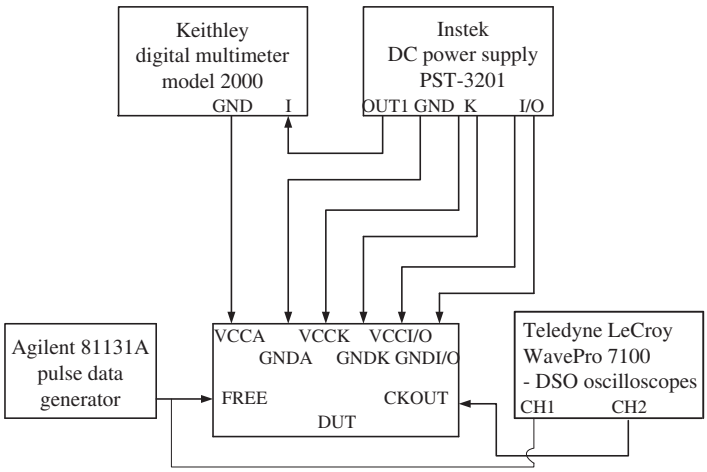

Figure 6 Setup for the experimental measurements.

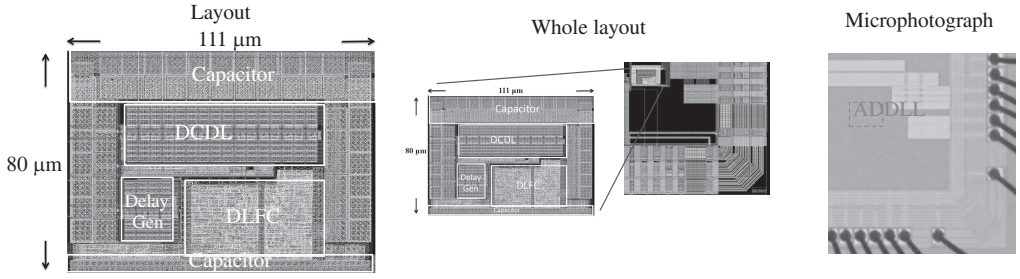

Figure 7 (a) Layout and (b) microphotograph of the fabricated chip.

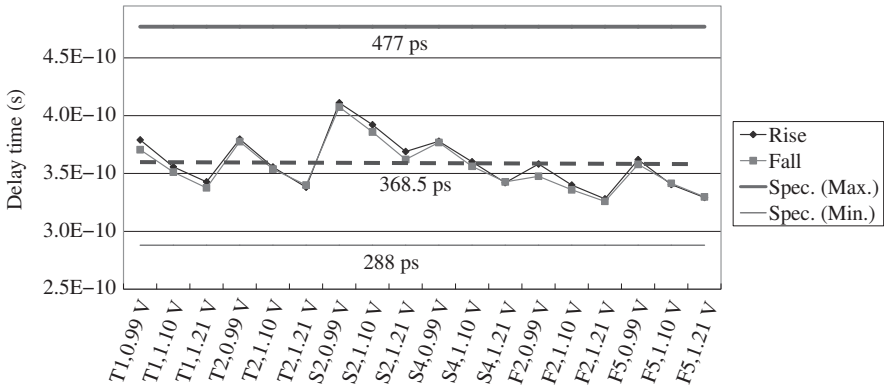

Figure 8 Measured phase shift error variations of output clock at 800 Mhz.

supply voltage at 1.1 V about 6 ps and 11 ps with respect to the rising and falling phase delays (from DQS to DQSD) is closest to the ideal value 368.5 ps.

The measured peak-to-peak and rms jitters of output clock for different operating frequencies versus the output frequency are shown in Figure 9 (a) and (b). The output jitter variation is plotted on a graph of different output frequency from 333 to 800 MHz (x-axis) versus jitters (y-axis). Fifteen voltage and temperature conditions for every sample are measured at 800 MHz and the best condition is found at 1.1 V, 0°C. The jitter values measured at 800 MHz (FREF) are 64.5 ps (peak-to-peak) and 7.8 ps (rms) of the 90-degree phase shift signals. Table 1 summarizes the performance of proposed ADDLL compared with previous reported works for DDR SDRAM application. It proves that the proposed ADDLL takes advantages of a novel DCDL scheme and integral sub-micron process technology in active area and power consumption.

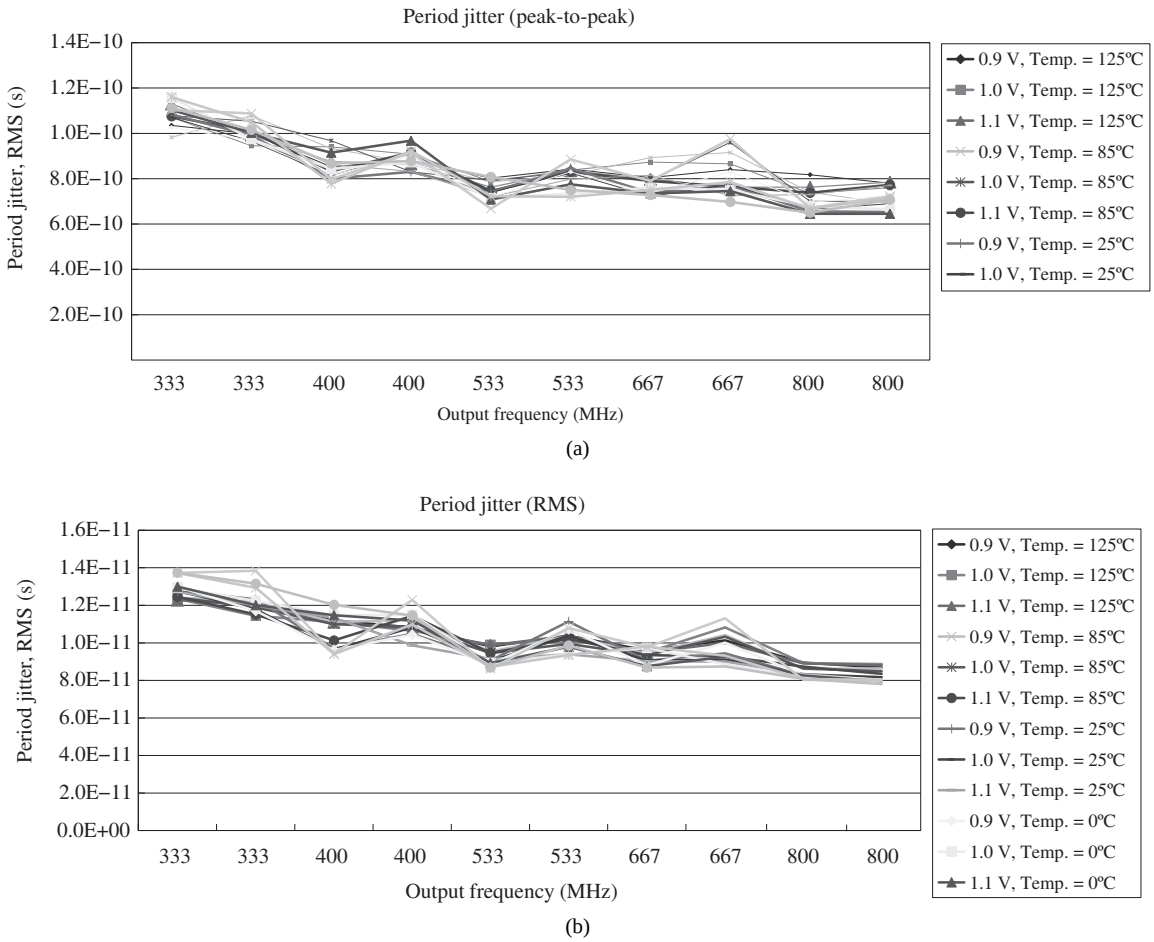

Figure 9 Measured variations of (a) peak-to-peak jitters (b) rms jitters at the output clock versus different output frequencies.

Table 1 Performance comparison with prior works

	Ref. [16]	Ref. [17]	Ref. [18]	Ref. [3]	Ref. [4]	This work
Type			All-Digital DLL			
Tech. (nm)	130	130	130	44	45	40
Supply voltage (V)	1.2	1.2	1.2	1.5	1.1	1.1
Operation range (MHz)	333–800	133–500	400–800	1.1GHz	400–800	333–800
Phase error (ps)	6.94				1.49–2.9	6–11
RMS jitter (ps)	2.95	10.3	2.6		2.17	7.8
Peak-to-peak jitter (ps)	22.2		19.1	45.6	17.8	64.5
Power (mW)	19.2	5.2	3.84	4.1	3.3	1.87
Area (mm^2)	0.0624	0.021	0.02	0.0176	0.01	0.0088

4 Conclusion

A low-power and area-efficient ADDLL with a 90-degree phase-shift was successfully implemented. A new DCDL scheme inside the DLL loop with adjusting techniques and improved hierarchical delay line architecture are presented in this paper. The fabricated chip used a 40-nm CMOS process with a supply voltage of 1.1 V and exhibited the ADDLL data rate range of 667 Mbps–1.6 Gbps which is suitable for high-frequency DDR3 SDRAM. Post-Layout simulations show that the actual 90° delay values between DQS1 and DQSD1 are close to the respective theoretical value. Measurements confirmed that the RMS jitter, the peak-to-peak jitter and the phase-shifter output of the ADDLL are 7.8, 64.5 and 6 ps, respec-

tively, at 1.6 Gbps DDR3 interface. The total power consumption of the ADDLL is 1.87 mW at 800 MHz. The active chip area of the test chip is 0.0088 mm^2.

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